REMARKS

Claims 2-6 and 23-29 are pending in the present application. Replacement claims 2-6, 23 and 24 are presented herewith. Claims 25-29 are also presented herewith. Claims 1, 7-9 and 19-22 have been canceled.

Information Disclosure Statement

The Examiner has alleged that the Information Disclosure Statement filed on September 17, 1999, fails to comply with 37 C.F.R. §1.98(a)(3), because it does not include a concise explanation of the relevance of the non-English language document. Accordingly, the document has not been considered.

However, as set forth in 37 C.F.R. §1.98(a)(3), "The concise explanation may be either separate from the specification or incorporated therein" (our emphasis added). Applicant respectfully submits that the concise explanation of the non-English language document "Semiconductor World", as cited in the Information Disclosure Statement filed on September 17, 1999, is provided on page 1 of the present application. Applicant therefore respectfully submits that the Information Disclosure Statement filed on September 17, 1999 is in compliance with 37 C.F.R. §1.98(a)(3).

Accordingly, the Examiner is respectfully requested to consider the non-English language document "Semiconductor World", in view of the concise explanation on page 1 of the present application, and to cite this corresponding docum nt of record in the present application, in accordanc with 37 C.F.R.

§1.98(a)(3).

Applicant also further respectfully notes that an Information Disclosure Statement has been filed in connection with the present application on January 28, 2002. The documents cited in this Information Disclosure Statement have been cited in parent application serial no. 09/342,751.

The Examiner is respectfully requested to acknowledge receipt of the Information Disclosure Statement filed on January 28, 2002, and to confirm that the corresponding documents have been considered and will be cited of record in the present application. Applicant also notes that all of the documents cited in parent application serial no. 09/342,751, have now been submitted in the present application.

Claim Rejections-35 U.S.C. 112

Claim 22 has been rejected under 35 U.S.C. 112, second paragraph, for the reasons stated on page 3 of the current Office Action. Claim 22 has been canceled. The Examiner is therefore respectfully requested to withdraw this rejection.

Claim Rejections-35 U.S.C. 103

Claims 1-9 and 19-24 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art and the Doan et al. reference (U.S. Patent No. 5,946,595), in further view of the Besser et al. reference (U.S. Patent No.

6,165,903). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

Applicant respectfully submits that the Examiner has not clearly establish on the record motivation for combining the prior art as relied upon, particularly the Doan et al. reference and Applicant's prior art Figs. 1A-1C. The Doan et al. reference is directed to forming local interconnects 34 of patterned titanium silicide. As can be seen in Fig. 11 of the Doan et al. reference, the local interconnect 34 is formed on top of the structure, above substrate 10. In contrast, Applicant's prior art Figs. 1A-1C is directed to a salicide process of a SOI type of semiconductor device. Particularly, the gate and source/drain regions are salicided, to provide a thin device. One of ordinary skill, looking to improve the semiconductor device of Applicant's prior art Figs. 1A-1C to be thin, would have no motivation to look to the Doan et al. reference, which is primarily concerned with forming local interconnects. Particularly, Applicant's prior art Figs. 1A-1C do not include local interconnects, and thus is not clear how the teachings should be combined, even if motivation for doing so existed. Accordingly, Applicant respectfully submits that this rejection, insofar as it may pertain to the presently pending claims, is improper for at least these reasons.

The method for fabricating a semiconductor device of claim 24 includes in combination doping an impurity into the supplemental silicon layer, and performing a second annealing to convert the first-reacted silicide region into a second-reacted silicide region, by reaction of the supplemental silicon layer with the first-reacted silicide

region. The semiconductor device is featured as including a p-channel MOS transistor having p-type source and drain diffusion layers, and an n-channel MOS transistor having n-type source and drain diffusion layers. The doping is featured as comprising "doping a p-type impurity into the supplemental silicon layer that is formed over the p-channel MOS transistor and doping an n-type impurity into the supplemental silicon layer that is formed over the n-channel MOS transistor". Applicant respectfully submits that these features would not have been obvious in view of the prior art as relied upon by the Examiner.

The prior art as relied upon by the Examiner does not disclose a structure including both a p-channel MOS transistor and an n-channel MOS transistor. Consequently, the prior art as relied upon by the Examiner does not disclose or even remotely suggest doping a p-type impurity into a supplemental silicon layer that is formed over a p-channel MOS transistor, and doping an n-type impurity into a supplemental silicon layer that is formed over an n-channel MOS transistor. Applicant therefore respectfully submits that the method of claim 24 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claim 24 is improper for at least these reasons.

With further regard to this rejection, as acknowledged by the Examiner on page 4, lines 5-6 of the Office Action dated October 2, 2001, Applicant's prior art Figs. 1A-1C and the Doan et al. reference do not disclose a supplemental silicon layer provided over a first-reacted silicide region. Accordingly, Applicant's admitted prior art and the Doan

et al. reference does not disclose or even remotely suggest doping a supplemental silicon layer with an impurity, as in claim 24.

Applicant also respectfully submits that deposited silicon layer 46 as illustrated in Figs. 8 and 9 of the Besser et al. reference is not described or even remotely suggested as being doped with an impurity. Particularly, column 5, line 25 through to column 6, line 12 of the Besser et al. reference does not describe or suggest doping deposited silicon layer 46 with an impurity. Accordingly, Applicant respectfully submits that the method of fabricating a semiconductor device of claim 24 distinguishes over and would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claim 24 is improper for at least these additional reasons.

Claims 25-29

Applicant respectfully submits that claims 25-29, as dependent upon claim 24, distinguish over and would not have been obvious in view of the prior art for at least similar reasons given with respect to claim 24, and by further reason of the features therein.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

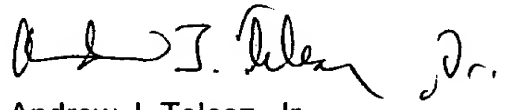
In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of one (1) month to February 2, 2002, for the period in which to file a response to the outstanding Office Action. The required fee should be charged to our Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

VOLENTINE FRANCOS, P.L.L.C.



Andrew J. Telesz, Jr.
Registration No. 33,581

AJT:cej

VOLENTINE FRANCOS, P.L.L.C.
12200 Sunrise Valley Drive, Suite 150
Reston, Virginia 20191
Telephone No.: (703) 715-0870
Facsimile No.: (703) 715-0877

Enclosures: Version with marked-up changes
Information Disclosure Statement dated January 28, 2002

VERSION WITH MARKED-UP CHANGES

Additions/Deletions to the Claims:

2. (Twice Amended) The method according to claim [1] 23, wherein the [material] metal layer comprises cobalt (Co).

3. (Twice Amended) The method according to claim [1] 23, wherein the [material] metal layer comprises titanium (Ti).

4. (Twice Amended) The method according to claim [1] 23, wherein the supplemental silicon layer is poly-silicon formed by a CVD (Chemical Vapor Deposition) technique.

5. (Twice Amended) The method according to claim [1] 23, wherein the supplemental silicon layer is a-Si (amorphous silicon) formed by a sputtering technique.

6. (Twice Amended) The method according to claim [1] 23, further comprising:

selectively removing non-reacted silicon from the second-reacted silicide region after the second [RTA process] annealing.

23. (Amended) A method for fabricating a semiconductor device, comprising:

providing a semiconductor substrate which has a silicon region located on [a] an

insulating layer formed in the semiconductor substrate;

forming a metal layer on the silicon region;

performing a first annealing to form a first-reacted silicide region;

forming a supplemental silicon layer on the first-reacted silicide region; and

performing a second annealing to convert the first-reacted silicide region into a second-reacted silicide region, by reaction of the supplemental silicon layer with the first-reacted silicide region,

wherein after the second annealing, a silicon layer remains between the second-reacted silicide region and the insulating layer.

24. (Amended) A method for fabricating a semiconductor device, comprising:

providing a semiconductor substrate which has a silicon region located on [a] an insulating layer formed in the semiconductor substrate;

forming a metal layer on the silicon region of the semiconductor substrate;

performing [on] a first annealing on the semiconductor substrate to form a first-reacted silicide region;

forming a supplemental silicon layer on the first-reacted silicide region;

doping an impurity[, which is a same conductive type as the silicon region,] into the supplemental silicon layer; and

performing a second annealing to convert the first-reacted silicide region into a second-reacted silicide region, by reaction of the supplemental silicon layer with the first-reacted silicide region.

the semiconductor device including a p-channel MOS transistor having p-type source and drain diffusion layers, and including an n-channel MOS transistor having n-type source and drain diffusion layers,

said doping comprising doping a p-type impurity into the supplemental silicon layer that is formed over the p-channel MOS transistor and doping an n-type impurity into the supplemental silicon layer that is formed over the n-channel MOS transistor.